What is claimed is:

1. A decoupling capacitor formed on an integrated circuit, the capacitor comprising:

first and second electrodes separated by a dielectric material;

a source positioned proximate to the first electrode; and

a floating drain positioned proximate to the first electrode and separated from the source by the first electrode, wherein the floating drain enhances an ability of the decoupling capacitor to withstand electrostatic discharges.

2. The decoupling capacitor of claim 1 wherein the decoupling capacitor comprises a plurality of capacitors.

3. The decoupling capacitor of claim 2 wherein the plurality of capacitors are arranged to form a multi-fingered structure.

4. The decoupling capacitor of claim 1 wherein the decoupling capacitor is fabricated using a metal oxide semiconductor technology.

5. The decoupling capacitor of claim 4 wherein the source is grounded and connected to a guard ring.

6. The decoupling capacitor of claim 1 further comprising a parasitic element formed by current interactions between the source, the floating drain, and a doped area.

7. The decoupling capacitor of claim 6 wherein the parasitic element functions as a bipolar junction transistor (BJT), and wherein the floating drain provides a constant potential region at the base of the BJT.

8. The decoupling capacitor of claim 6 wherein the doped area is a source for another capacitor.

9. A multi-fingered decoupling capacitor with electrostatic discharge resistance formed on an integrated circuit, the decoupling capacitor comprising:

a first finger comprising:

first and second electrodes separated by a dielectric material; and

a first source positioned proximate to the first electrode;

a second finger comprising:

third and fourth electrodes separated by a dielectric material; and

a second source positioned proximate to the third electrode; and

a floating drain, wherein the floating drain is positioned proximate to the first and third electrodes and separated from the first source by the first electrode and from the second source by the third electrode, and wherein the floating drain enhances an ability of the decoupling capacitor to withstand electrostatic discharges.

10. The decoupling capacitor of claim 9 further comprising a parasitic element formed by current interactions between the first source, the floating drain, and the second source.

11. The decoupling capacitor of claim 10 wherein the parasitic element functions as a bipolar junction transistor (BJT), and wherein the floating drain provides a constant potential region at the base of the BJT to help distribute current more evenly between the first and second capacitors during snapback.

12. The decoupling capacitor of claim 9 wherein the decoupling capacitor is fabricated using a metal oxide semiconductor (MOS) technology.

13. The decoupling capacitor of claim 12 wherein the decoupling capacitor has a positive-channel MOS structure.

14. The decoupling capacitor of claim 12 wherein the decoupling capacitor has a negative-channel MOS structure.

15. The decoupling capacitor of claim 12 wherein each of the second and fourth electrodes are fabricated using a P+ polysilicon, and wherein each of the first and second fingers includes an N well thin oxide.

16. The decoupling capacitor of claim 9 wherein the second and fourth electrodes are connected to a voltage source.

17. The decoupling capacitor of claim 16 wherein the second and fourth electrodes are connected to the voltage source via a voltage pad, and wherein the floating drain reduces a susceptibility of the voltage pad to electrostatic discharges.

18. A method for fabricating a decoupling capacitor with increased resistance to electrostatic discharges on an integrated circuit, the method comprising:

forming a well region;

forming a gate oxide layer above the well region;

forming a polysilicon gate structure above the gate oxide layer;

forming a source region proximate to the gate oxide layer;

forming a drain region proximate to the gate oxide layer and opposite the source region;

covering the polysilicon gate structure, the source region, and the drain region with a dielectric layer; and

forming, through the dielectric layer, a first interconnection to the source region and a second interconnection to the polysilicon gate structure, while leaving the dielectric layer above the drain region intact, wherein the drain region is not connected to an interconnection and is floating.

19. The method of claim 18 further comprising:

forming a guard ring; and

connecting the source region to the guard ring.

20. The method of claim 18 further comprising:

forming another polysilicon gate structure for a second decoupling capacitor; and

connecting the polysilicon gates with a polysilicon line, so that the two decoupling capacitors are combined into a single decoupling capacitor.